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CSE 310

**Homework 1**

1. Explain what a Von Neumann Computer is.

* A Von Neumann Computer is a fundamental model of a computer for processing computer programs. The model consists of 5 parts:
  1. Memory (MU)
  2. Processing Unit (CU + ALU)
  3. Input (Keyboard, Mouse, Disks, etc.)
  4. Output (Monitor, Printer LED, Disks, etc.)
  5. Control Unit (CU)

1. Convert the binary number **10101.11011011** to octal.
   * + *010 101 = 25*
     + 011 011 011 = 333

1. Convert the decimal number **2429.625** to octal.

1. Convert the decimal number **532.97** to octal.

1. Convert the binary number **0.0110111** to hexadecimal.

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=

* .875 \* 16 = 14.0 = E

1. Determine the value of base x if

1. Convert the hexadecimal number **F3A7C2** to octal.

1. Convert the binary number to decimal: **1110101.101**.

1. Write a Verilog module that implements the following Boolean equation:

f1 = a \* b \* c' + a \* c + c

Simplify the above expression; write another module to implement it as f2.

Write a test bench to check whether f1 and f2 are identical with different values of *a, b,* and *c*.

*boolean.v:*

// f1 = a \* b \* c' + a \* c + c

module boolean1( output F1, input A, input B, input C );

assign F1 = A && B && !C || A && C || C;

endmodule

// f2 = ( a \* b ) + c

module boolean2( output F2, input A, input B, input C );

assign F2 = ( A && B ) || C;

endmodule

*boolean\_test.v:*

// 'include "boolean\_test.v"

module testBoolean();

reg A, B, C;

wire F1, F2;

// Intialize all variables

initial begin

$display ("time\t A B C F1 F2");

$monitor ("%g\t %b %b %b %b %b", $time, A, B, C, F1, F2);

A = 0;

B = 0;

C = 0;

#75 $finish;

end

always begin

#5 C = ~C;

end

always begin

#10 B = ~B;

end

always begin

#20 A = ~A;

end

boolean1 test1( .F1(F1), .A(A), .B(B), .C(C) );

boolean2 test2( .F2(F2), .A(A), .B(B), .C(C) );

endmodule

~

Sample Inputs:

A = 0

B = 0

C = 0

Sample Output:

**$** ./boolean\_test

time A B C F1 F2

0 0 0 0 0 0

5 0 0 1 1 1

10 0 1 0 0 0

15 0 1 1 1 1

20 1 0 0 0 0

25 1 0 1 1 1

30 1 1 0 1 1

35 1 1 1 1 1

40 0 0 0 0 0

45 0 0 1 1 1

50 0 1 0 0 0

55 0 1 1 1 1

60 1 0 0 0 0

65 1 0 1 1 1

70 1 1 0 1 1

75. 1 1 1 1 1

Sample Inputs:

A = 1

B = 0

C = 1

Sample Outputs:

**$** ./boolean\_test

time A B C F1 F2

0 1 0 1 1 1

5 1 0 0 0 0

10 1 1 1 1 1

15 1 1 0 1 1

20 0 0 1 1 1

25 0 0 0 0 0

30 0 1 1 1 1

35 0 1 0 0 0

40 1 0 1 1 1

45 1 0 0 0 0

50 1 1 1 1 1

55 1 1 0 1 1

60 0 0 1 1 1

65 0 0 0 0 0

70 0 1 1 1 1

75. 0 1 0 0 0

**Discussion**: I completed all the questions that were asked and showed my work for each question. I will give myself 50/50.